VPX56-3HU
3U AC Input VPX Power Line Conditioner with Holdup
Up To 400 Watts, Ruggedized
VITA Front End Plug-in Module, Conduction-Cooled

Made in the USA
Certified Small Business

Description

NAI's VPX56-3HU is a 400 Watt AC/DC power Line Conditioner which accepts a 3 Phase AC input and plugs directly into a standard 3U VPX chassis with a VITA 62.1, 1.0" power supply slot. This off-the-shelf solution is compatible with VPX specifications.

The VPX56-3HU power line conditioner provides holdup capability and protects downstream DC-DC converters from Mil-Std 704 transients, low voltage conditions and power interruptions; providing up to 50 milliseconds of holdup time at up to 400 watts. The VPX56-3HU is designed to meet standard 3U VPX (VITA62) mechanical requirements and is a perfect companion unit for all NAI VPX +28Vdc DC/DC converters. This COTS conditioner is specifically designed with NAVMAT component derating for rugged defense and industrial applications. It is also designed to meet the many harsh environmental requirements of military applications.

Features

- Ideal for rugged 3U VPX power applications
- Standard VPX-compatible connector per VITA 62
- Compatible with System Management Bus per VITA 46.11
- Off-the-shelf solution for VITA 46.0 and VITA 65 systems
- Supports all VITA standard I/O, signals, and features
- Protects DC/DC Converters from Mil-Std 704F Transients
- Designed to work with the NAI VPX55-3 family of DC-DC Converters
- VITA 62.1 Connectors and Spacers
- Wedgelock, Plug-in Design (conduction cooled)
- Holdup
- Standby Output
- BIT

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Electrical Specifications

DC Input Characteristics	
Input	115Vac, Three Phase AC Input
Input Voltage Range	±10%
Frequency Range	360Hz to 440Hz
EMI/RFI	Per MIL-STD-461F when used with additional system EMI filtering.
Input Transient Protection	Per MIL-STD-704F Ride through protection for: Normal Voltage Transients & Power Interrupts
Power Factor	0.85 minimum
Main DC Output Power	Provides 40Vdc @ 400 watts maximum to downstream NAI DC/DC Converters.
Holdup Time	Up to 400 watts of primary power for up to 50millisecond.
Holdup Cap Replenishment Time	500 milliseconds
Efficiency	92% Typical
HU_FAIL*	Indicates internal failure within the unit. Signal complies with VITA 65 for active Low. FAIL* signal is Open Drain. It is expected that there will be a pull-up resistor on the backplane.
HU_ENABLE*	Turns off all of the output voltages, including AUX, when signal is High. ENABLE* can be pulled Low by using a mechanical switch or other means which connects it to SIGNAL_RETURN. A Logic output can also be used to drive the ENABLE*. Opening the switch would turn off all the outputs; closing the switch or applying the Logic output would enable the outputs to come on depending on the state of INHIBIT*. An input of <1.0 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with INHIBIT*, this signal determines the output power status of the VPX55-3 (see Power Status Table below).
HU_INHIBIT*	Turns off the output voltage. The signal does not affect the 3.3 V_AUX. Pulling INHIBIT* Low turns off power to back end modules. An input of <1.0 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with ENABLE*, this signal determines the output power status of the VPX55-3 (see Power Status Table below).
Geographical Addressing	As defined in VITA 46.
Protocol	Per VITA 46.11 System Management Bus.

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Physical/Environmental Specifications	
Temperature Range	Operating: -40°C to +85°C at 100% load (temperature measured at card edge, conduction via card edge); Storage: -55°C to +100°C per VITA 47 CC4)
Reliability (MTBF)	100,000 hours, Ground Benign at 50°C Baseplate
Altitude	1,400 feet (below sea level) to +60,000 feet per VITA 47
Shock	30 G's each axis per MIL-STD-810G, Method 516.6, Procedure 1; Hammer shock per MIL-S 901, ½ sine wave per VITA 47 OS2
Acceleration	6 G's per MIL-STD-810G, Method 513.6, Procedure II
Vibration	Per MIL-STD-810G, Method 514.6, Procedure 1A
Humidity	95% at 71°C per MIL-STD-810G, Method 507.5 (non-condensing)
Salt & Fog	Per MIL-STD-810G, Method 509.5
Sand/Dust	Per MIL-STD-810G, Method 510.5
Fungus	Per MIL-STD-810G, Method 508.6
ESD	15 kV EN61000-4-2 per VITA 47
Enclosure	Aluminum housing to aluminum baseplate
Dimensions	Standard 3U, VITA 62, Single Card Slot 1.0" See Mechanical Layout
Finish	Chemical film IAW MIL-DTL-5541, Type II, Class 3
Interface	50 Micro-Inch Gold on contacts; plated tails for tin whisker mitigation; See Connector Part Numbers below
Weight	1.5 LBS TYPICAL (STD 1.0" Pitch)

All specifications are subject to change without notice.

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LED Status

LED State	Meaning
Off	Input out of nominal range
Green (Steady)	All outputs are good
Red (Steady)	Fail; Follows same logic as HU_FAIL * signal
Blinking Green	Unit disabled
Blinking Red	Over Voltage or Over Temperature (all outputs are off)

Power Status

Control Input States		Power Output States	
ENABLE*	INHIBIT*	+3.3V_AUX	Output
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

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I²C Communication

Description

I²C is a bi-directional, two wire serial bus which provides communication using a data line and clock line (SDA and SCL).

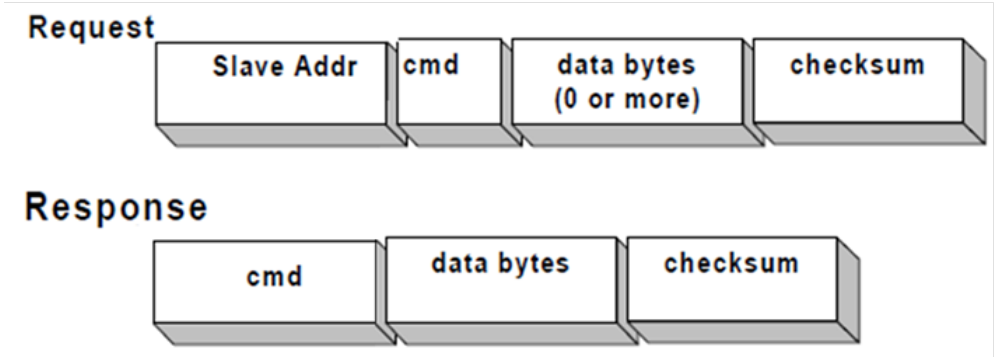
Using I²C Communication on NAI, VPX Series Power Supplies

1. Hardware Interface.
   Electrical interface is based on I2C parameters at 100 kHz. The backplane or I2C master controller should provide pull up resistors on SDA (Data) and SCL (Clock) lines to a 3.3V rail. On the NAI **VPX Series,** the SDA line is located on Pin D5 (SM1) and the SCL line is located on pin C5 (SM0).

2. Address.
   The I2C Address is 7 bits. Default base address is 0x20. *GA0, and *GA1 provides 2 LSB's for the address.
   The *GA pins have pull-up resistors internal to the power supply to 3.3V. When left open, the address will be 0x20, with both grounded the address will be 0x23, see table below.

Pin		I2C Address
*GA1	*GA0	
Pin - B5	Pin - A5	
High	High	0x20
High	Gnd	0x21
Gnd	High	0x22
Gnd	Gnd	0x23

1. **Data Read - Get Sensor Reading results**



	Byte	Data Field	Data
Request Data	1	cmd	See table
	2 to n-1	Data If Required by cmd or Zero ChkSum* if no Data required.	
	n	Zero ChkSum* if Data was required by cmd	
Response Data	1	Completion Code – Echo cmd Number	
	2 to n-1	Per cmd Response	
	n	Zero ChkSum	

Note : Slave address should not be included in Zero Checksum calculation.

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2. Commands

Sensor #	Name	Description
21H	Composite Sensor	64 bytes of scanned sensor data. Data is continually scanned and available for report. Data consists of 2 bytes of data for each of the 11 sensors and FRU data.
55H	Status Write Command	Writes Status byte on Composite Sensor.
44H	Firmware release date	22 byte response. Month/Day/Year Hr/Min/Sec in ASCII form.
45H	Hardware Address	3 byte response. Reports address set by GA0*-GA1*

4.1 Composite Sensor Read Command – 21H

Response BYTE #	Data Type	Meaning
0	Completion Code – 21h	Echo of the command
1	Status Register 0, MS Bit First	Refer to table below
2-3	Signed Integer, MSB First	Temperature as follows °C = (Reading * 100 / 16384)
4-5	U Integer, MSB First	Voltage on HU, 28V = 16384
6-7	U Integer, MSB First	Reserved
8-9	U Integer, MSB First	Reserved
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Reserved
14-15	U Integer, MSB First	Reserved
16-17	U Integer, MSB First	Current on HU, 10A = 16384
18-19	U Integer, MSB First	Reserved
20-21	U Integer, MSB First	Reserved
22-23	U Integer, MSB First	Reserved
24-25	U Integer, MSB First	Reserved
26-27	U Integer, MSB First	Reserved
28-29	U Integer, MSB First	Internal Reference, 2.5V = 16384
30-31	U Integer, MSB First	Rectified Input Bus, 270V = 16384
32-51	Character String	Part Number
52-53	U Integer, MSB First	S/N Hi
54-55	U Integer, MSB First	S/N Low
56-57	U Integer, MSB First	Date Code (Year/Week)
58-59	U Integer, MSB First	Hardware Rev
60-61	U Integer, MSB First	Firmware Rev.
62	Reserved	Reserved
63	Zero Checksum	Value required to make the sum of bytes 0 to 62 add to a multiple of 256 (decimal).

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Status Reg 0		R/Set	R/Set	R/W	R/W	R/W	R	R
Bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.

Bits 3 and 2 (SWInh SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

4.2 Status Write Command - 55H

BYTE #	Data Type	Meaning
0	U Character – 55H	Command
1	U Character	Data
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

The command to write to Status byte is 55h, followed by 8-bit data then zero checksum.

Example: To send a command to clear the faults and turn on all the outputs, the following sequence must be sent.
55h 78h 33h;

55h is the command needed to write to status byte zero.
78h data for byte zero,

Bit 7 set: don't care bit.
Bit 6 set: FAIL signal is high, software will clear it if unit fails
Bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.
Bit 4 set: Software has priority to enable/disable unit.
Bit 3 set: SWInhibit is high
Bit 2 low: SWEnable is low.

33h Value to achieve a sum of zero.

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4.3 Firmware release date – 44H

Response BYTE #	Data Type	Meaning
0	Completion Code – 44H	Echo of the command
1-20	Character String	Date
21	Zero Checksum	Value required to make the sum of bytes 0 to 20 add to a multiple of 256 (decimal).

4.4 Hardware Address – 45H

Response BYTE #	Data Type	Meaning
0	Completion Code – 45H	Echo of the command
1	U Character	I2C Hardware Address
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

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Pinout Designations (P1)

Pin Number	Rated Current (A)	Pin Name	Description
LP1	20A	Phase A	Input
LP3	20A	Phase B	Input
LP5	20A	Phase C	Input
LP7	20A	Neutral	Input Neutral
LP9	20A	Hold Up+	Can be used to connect to an external energy storage module. If not used, this is not connected.
LP11	20A	Hold Up-	Can be used to connect to an external energy storage module. If not used, this is not connected.
LP13	20A	Chassis	
A1	<1A	GA0*	Geographical Address 0
A2	<1A	GA1*	Geographical Address 1
A3	<1A	UD0	User Defined
B1	<1A	SM0	I^2C Clock
B2	<1A	SM1	I^2C Data
B3	<1A	SM2	For 2nd I^2c Bus (not Currently Implemented)
C1	<1A	SM3	For 2nd I^2c Bus (not Currently Implemented)
C2	<1A	Inhibit*	Used to turn off Main Output Power; Leaves +3.3Vdc_Aux on
C3	<1A	Fail*	Active Low, Open Drain
D1	<1A	Signal_Return	Common Signal & Aux Output Return
D2	<1A	Enable*	Used to turn off Main Output Power and +3.3Vdc_Aux
D3	<1A	3.3V_Aux	Auxiliary Low Power Output
P1	40A	V Out	Output Voltage to DC/DC Converter
P2	40A	V Out Return	Output Voltage Return to DC/DC Converter

VITA 62.1 Connectors

Connector	Backplane vs. Plug-In Module	TE Connectivity
P0	Plug-In Module	2332793-1
J0	Backplane	2332795-1

*mating connector not included

VITA 62.1 Separators

Connector	Backplane vs. Plug-In Module	TE Connectivity
P0	Plug-In Module	2313445-1
J0	Backplane	2313444-1

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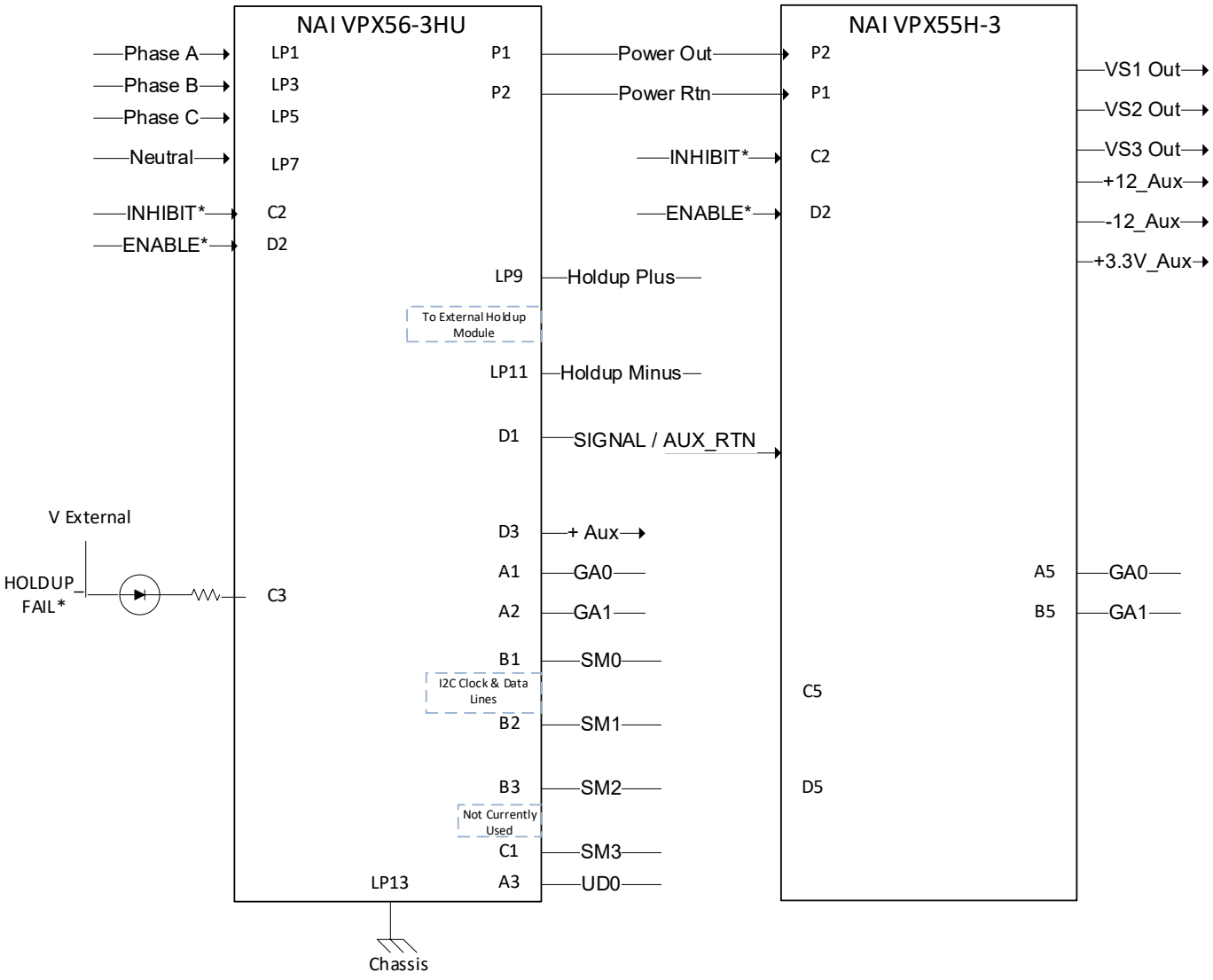
VPX56-3HU Connections



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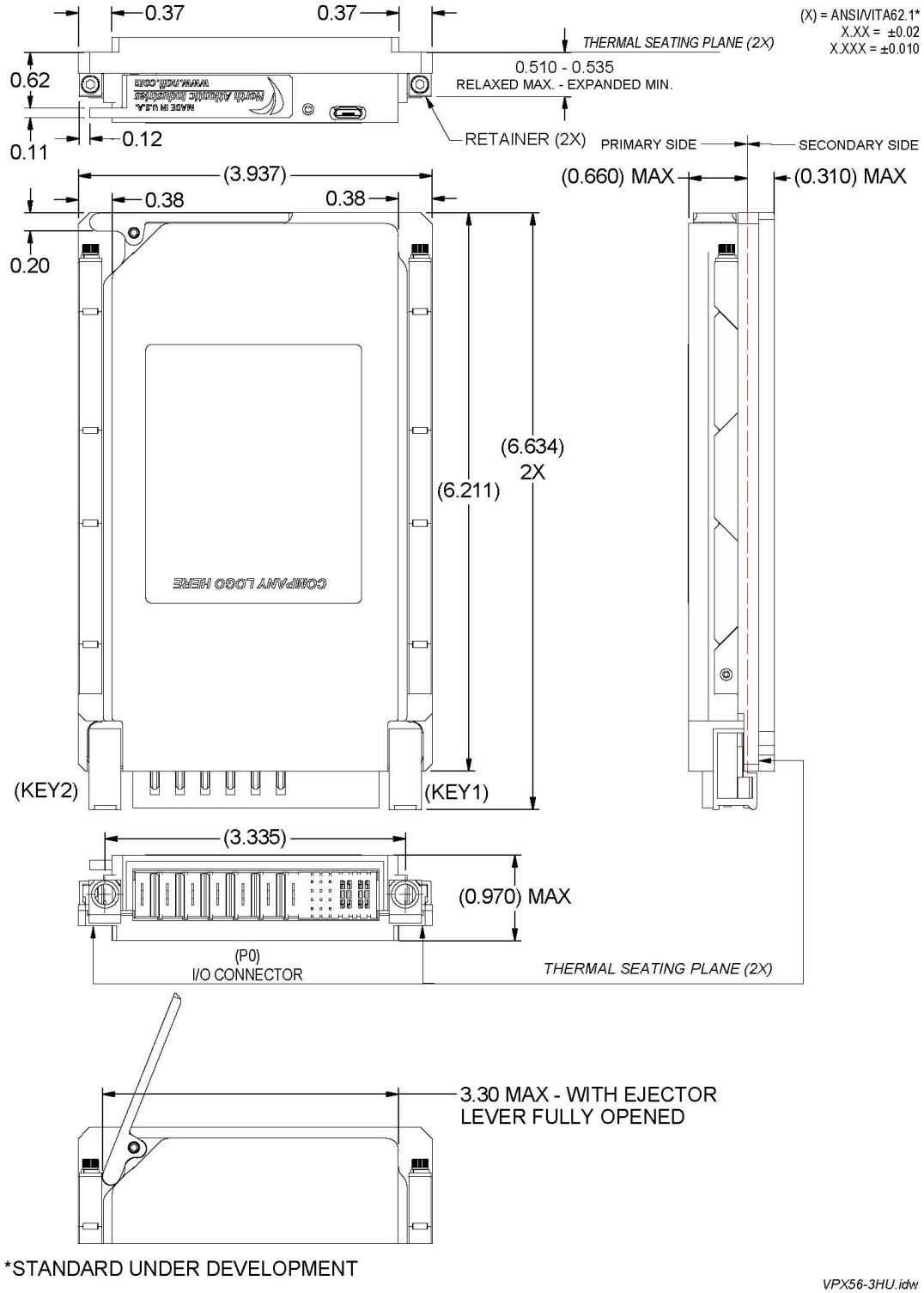
Mechanical Layout



*STANDARD UNDER DEVELOPMENT

VPX56-3HU.idw

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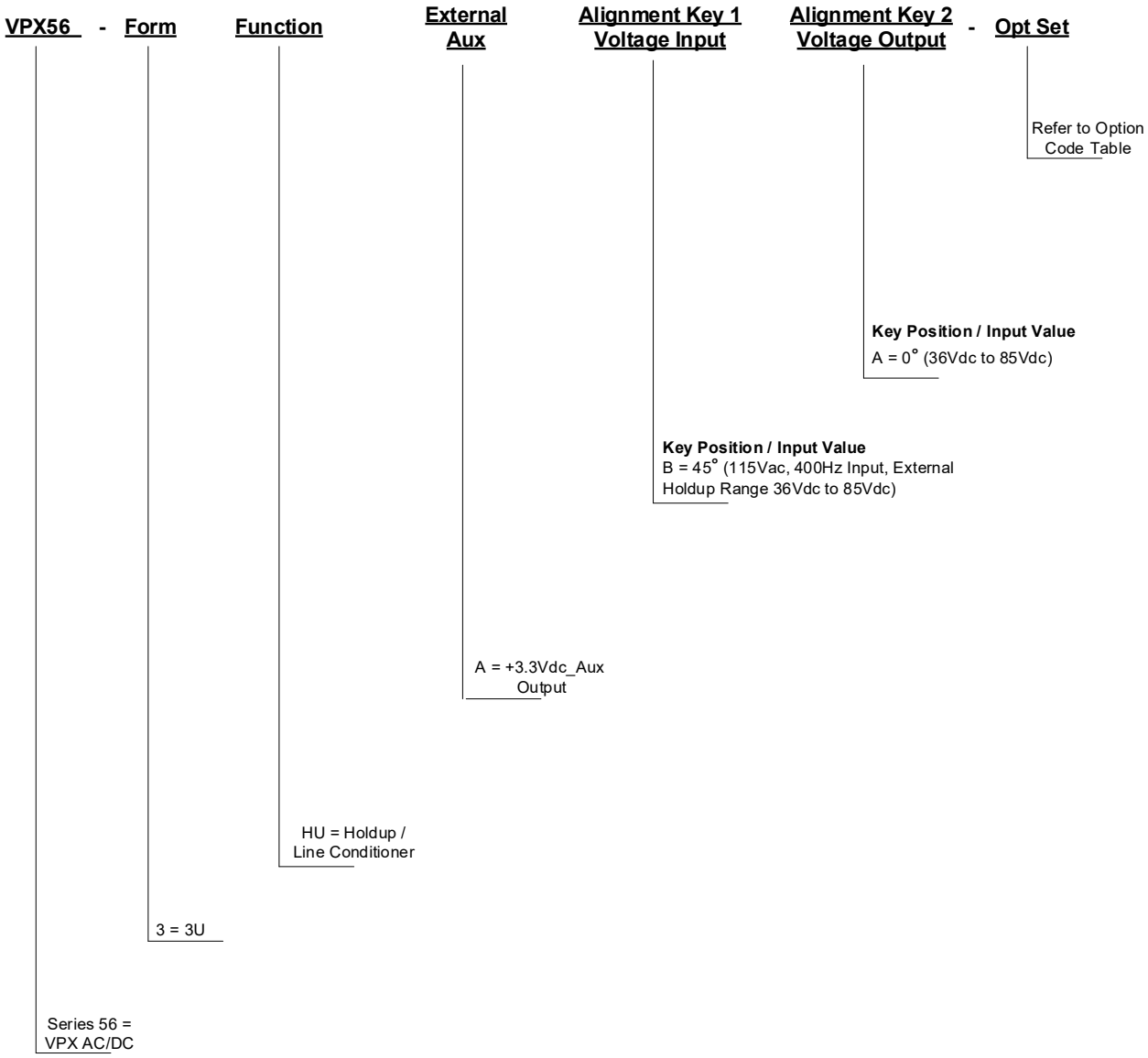
Ordering Information



Example Part Number:
VPX56-3HUABA-00 = 3U VPX AC/DC Power Line Conditioner with Holdup, 1.0" pitch, up to 400 Watts, no additional options

Refer to option code table for description of option codes

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Option Code Table

Code	Description
00	Standard unit, no additional options
01	Holdup Power of 325 Watts @ 85°C, Holdup Capacitor Replenishment time is 500 milliseconds

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