VPX68S 3U VPX DC/DC Converter

600-Watt Ruggedized Converter
Developed in alignment with the SOSA™ Technical Standard
Plug-in Module, Conduction-Cooled, SOSA™, With Holdup Time

Made in the USA
Certified Small Business

Description

NAI's VPX68S-3 is a 600 Watt DC/DC Converter which plugs directly into a standard 3U VPX chassis with a VITA 62, 1.0" pitch power supply slot. This off-the-shelf solution for VITA 46.0 and VITA 65 systems is compatible with VPX specifications; supports all VITA standard I/O, signals, and features; and conforms to the VITA 62 mechanical and electrical requirements for modular power supplies.

The VPX68S-3 switching power supply is conduction-cooled through the card edge/wedgelock. It accepts +28 VDC input voltage and provides two SOSA™ outputs at up-to 600 Watts and has Optional, integrated Holdup Time.

The VPX68S-3 supports a variety of standard features, including continuous Background Built-in-Test (BIT); remote error sensing; and protection against transients, over-voltage, over-current, and short-circuits. With its intelligent design, the VPX68S-3 also has the flexibility to address special needs. This COTS converter is specifically designed with component derating for rugged defense and industrial applications. It is also designed to meet the many harsh environmental requirements of military applications.

Electrical Specifications

Features

- Ideal for rugged 3U VPX power applications
- Standard VPX-compatible connectors and I/O per VITA 62
- IPMI Dual PM Bus compliant
- Supports all VITA standard I/O, signals, and features
- Accepts +28 VDC input
- Provides SOSA outputs and I/O at up-to 600 Watts
- High Efficiency
- Continuous Background Built-in-Test (BIT)
- Current Share (optional)
- Holdup Time
- Input transient protection per MIL-STD-704F
- Input Protection per MIL-STD-1275E
- Integrated EMI filtering per MIL-STD-461F
- Environmentals per MIL-STD-810G and VITA 47
- Operates at full load through the entire -40°C to +85°C temp range

DC Input Characteristics

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Input	+28 VDC (+16 VDC to +60 VDC range, continuous)
EMI/RFI	Designed to meet the requirements of MIL-STD-461F; CE102 standalone compliant (**without** additional filtering)
Input Transient Protection	Per MIL-STD-704F - Meets 704F Normal, Abnormal and Emergency Steady State input - Rides through 704F Normal and Abnormal high voltage transients - Rides through 704F Normal low voltage transients. Will not be damaged and will automatically restart from 704F abnormal transients and power interruptions
	Per Mil-Std-1275E 250Vdc Spike and 100Vdc Surge
Output Power	up-to 600 Watts max (see Output Power Table)
Output Voltage	VPX outputs standard (see Output Power Table)
Efficiency	92% typical
Switching Frequency	250KHz
Line Regulation	Within 0.5% or 20 mV (whichever is greater) for low to high line changes at constant load.
Load Regulation	0.5% or 20 mV (whichever is greater) for 0 to 100% of rated load at nominal input line with remote sense.
PARD (Noise and Ripple)	1% or 50 mV p-p max per VITA 62; measurements are made with a 20 MHz bandwidth instrument connected on load wires < 5 inches from power supply and terminated with 1uF capacitors across load lines
Load Transient Recovery	Output voltage returns to regulation limits within 0.5 msec
Load Transient Under/Overshoot	5% of nominal output voltage set point (1.4 V max); 2.5% for VS3
Holdup Time (optional)	Provides 50 milliseconds of Holdup Time at up-to 400 Watts
Short Circuit Protection	Protected for continuous short circuit with automatic recovery
Current Limiting	115% (min) to 145% (max) of rated load; will periodically retry until condition is removed
Over Voltage Protection	Automatic electronic shutdown if outputs exceed 125% ±10%
Remote Error Sensing	Sensing pins compensate for up to 0.5 V drop on VS1 to VS3 outputs
Isolation Voltage	250 VDC input to output and input to case; 100 VDC output to case
Insulation Resistance	50 Mega Ohm at 250 VDC

All specifications are subject to change without notice.

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Additional Specifications

Physical/Environmental	
Temperature Range	Operating: -40°C to +85°C at 100% load (temperature measured at card edge, conduction via card edge); Storage: -55°C to +105°C per VITA 47 CC4)
Temperature Coefficient	0.01% per °C
Shock	30 G's each axis per MIL-STD-810G, Method 516.6, Procedure 1; Hammer shock per MIL-S 901, ½ sine wave per VITA 47 OS2
Acceleration	6 G's per MIL-STD-810G, Method 513.6, Procedure II
Vibration	Per MIL-STD-810G, Method 514, Procedure 1
Humidity	95% at 71°C per MIL-STD-810G, Method 507.5 (non-condensing)
Altitude	1,500 feet below sea level to 60,000 feet above sea level per VITA 47
Salt & Fog	Per MIL-STD-810G, Method 509.5
Sand/Dust	Per MIL-STD-810G, Method 510.5
Fungus	Per MIL-STD-810G, Method 508.6
ESD	15 kV EN61000-4-2 per VITA 47
Enclosure	Aluminum housing to aluminum baseplate
Dimensions	See Mechanical Layout
Finish	Chemical film IAW MIL-DTL-5541, Type II, Class 3
Interface	50 Micro-Inch Gold on contacts; plated tails for tin whisker mitigation; See Connector Part Numbers below
Weight	2.2lbs, Typical

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Connectors

Unit	Backplane
P0: TE Connectivity p/n 2314578-2	**J0:** 2 TE Connectivity p/n 309390-1

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Signal Types

Signal	Description
ENABLE*	Turns off all of the output voltages, including 3.3 V_AUX, when signal is High. ENABLE* is pulled Low by using a mechanical switch which connects it to SIGNAL_RETURN. A Logic output can also be used to drive the ENABLE*. Opening the switch would turn off all the outputs; closing the switch or applying the Logic output would enable the outputs to come on depending on the state of INHIBIT*. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with INHIBIT*, this signal determines the output power status of the VPX68S-3 (see Power Status Table below).
INHIBIT*	Turns off all the output voltages. In most implementations, the signal is expected to leave 3.3 V_AUX on. Pulling INHIBIT* Low turns off VS1, VS2, VS3, and ±12 VDC_Aux outputs. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with ENABLE*, this signal determines the output power status of the VPX68S-3 (see Power Status Table below).
SYSRESET*	An active low open-collector line driven by the Power Monitor module. Signal ensures a clean, stabilized startup based on monitoring the output voltage levels in accordance with VITA 46.0, paragraph 4.8.11. Timing can be factory customized.
FAIL*	Indicates failure when any of the outputs are not within specification. Signal complies with VITA 65 for active Low. FAIL* signal is Open Drain. It is expected that there will be a pull-up resistor on the backplane.
VBAT (Optional)	Provides a low-power +3.3 VDC @ 1A output to other plug-in modules. Intent is to supply power to low current devices, such as Real Time Clocks, when other outputs are off. While connected internally to the +3.3 VDC_Aux output, the signal provides a separate line dedicated to low power needs and has its own overcurrent protection. The signal is controlled thru power status, along with the +3.3 VDC_Aux output (see Power Status Table below).
Geographical Addressing	As defined in VITA 46
Current Share	Allows multiple supplies to share system load for VS1-VS3 outputs. Connection per designated pins each output.
Protocol	IPMI Dual PMBus.
Status LED	6 State LED as shown below in LED Status Table

LED Status

LED State	Meaning
Off	Input Low
Green (Steady)	Vout OK; All outputs are good
Red (Steady)	Fail; Follows same logic as FAIL* signal
Blinking Green	Unit disabled
Blinking Red	Over Voltage or Over Temperature (all outputs are off)
Purple (Steady)	SYSRESET is enabled (Output(s) indicate a fault)

Power Status

Control Input States		Power Output States	
ENABLE*	INHIBIT*	+3.3V_AUX	VS1
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

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Output Power

+12V Only Configuration per SOSA™		
Designation (Power Form)	**Volts**	**Amps**
VS1 (PO1)	+12Vdc	50*
+3.3V_Aux	+3.3Vdc	20
VS1 (PO1)	+12Vdc	50*

***Total of 50Amps capability from P01 combined**

Pinout Designations (P0)

PIN #	RATED CURRENT (A)	Pin Name	12V Only SOSA™ Configuration	PIN #	RATED CURRENT (A)	Pin Name	12V Only SOSA™ Configuration
P1	40A	-DC_IN/ACN	-DC_IN/ACN	B5	<1A	GA1*	GA1*
P2	40A	+DC_IN/ACL	+DC_IN/ACL	C5	<1A	SM0	SM0
LP1	20A	CHASSIS	CHASSIS	D5	<1A	SM1	SM1
A1	<1A	UD1	SYNC_OUT (UD1)	A6	<1A	SM2	SM2
B1	<1A	UD2	NVMRO (UD2)	B6	<1A	SM3	SM3
C1	<1A	UD3	GA2* (UD3)	C6	<1.5A	-12V_AUX	Reserved
D1	<1A	UD4	UD4	D6	<1A	SYSRESET*	SYSRESET*
A2	<1A	VBAT	VBAT	A7	<1A	SHARE_1	SHARE_1
B2	<1A	FAIL*	FAIL*	B7	<1A	SHARE_2	SHARE_2
C2	<1A	INHIBIT*	INHIBIT*	C7	<1A	SHARE_3	SHARE_3
D2	<1A	ENABLE*	ENABLE*	D7	<1A	SIGNAL_RETURN	SIGNAL RETURN
A3	<1A	UD0	SYNC_IN (UD0)	A8	<1A	PO1_SENSE	SENSE, +12VDC
B3	<1.5A	+12V_AUX	Reserved	B8	<1A	PO2_SENSE	SENSE, 3.3V_AUX
C3	<1A	N/U	N/U	C8	<1A	PO3_SENSE	SENSE, +12VDC
D3	<1A	N/U	N/U	D8	<1A	SENSE_RETURN	SENSE RETURN
A4	<1.5A	3.3V_AUX	Reserved	P3	40A	PO3	+12VDC (Vs1)
B4	<1.5A	3.3V_AUX	Reserved	P4	40A	POWER_RETURN	POWER RETURN
C4	<1.5A	3.3V_AUX	Reserved	P5	40A	POWER_RETURN	POWER RETURN
D4	<1.5A	3.3V_AUX	Reserved	LP2	20A	PO2	3.3V_AUX
A5	<1A	GA0*	GA0*	P6	40A	PO1	+12VDC (Vs1)

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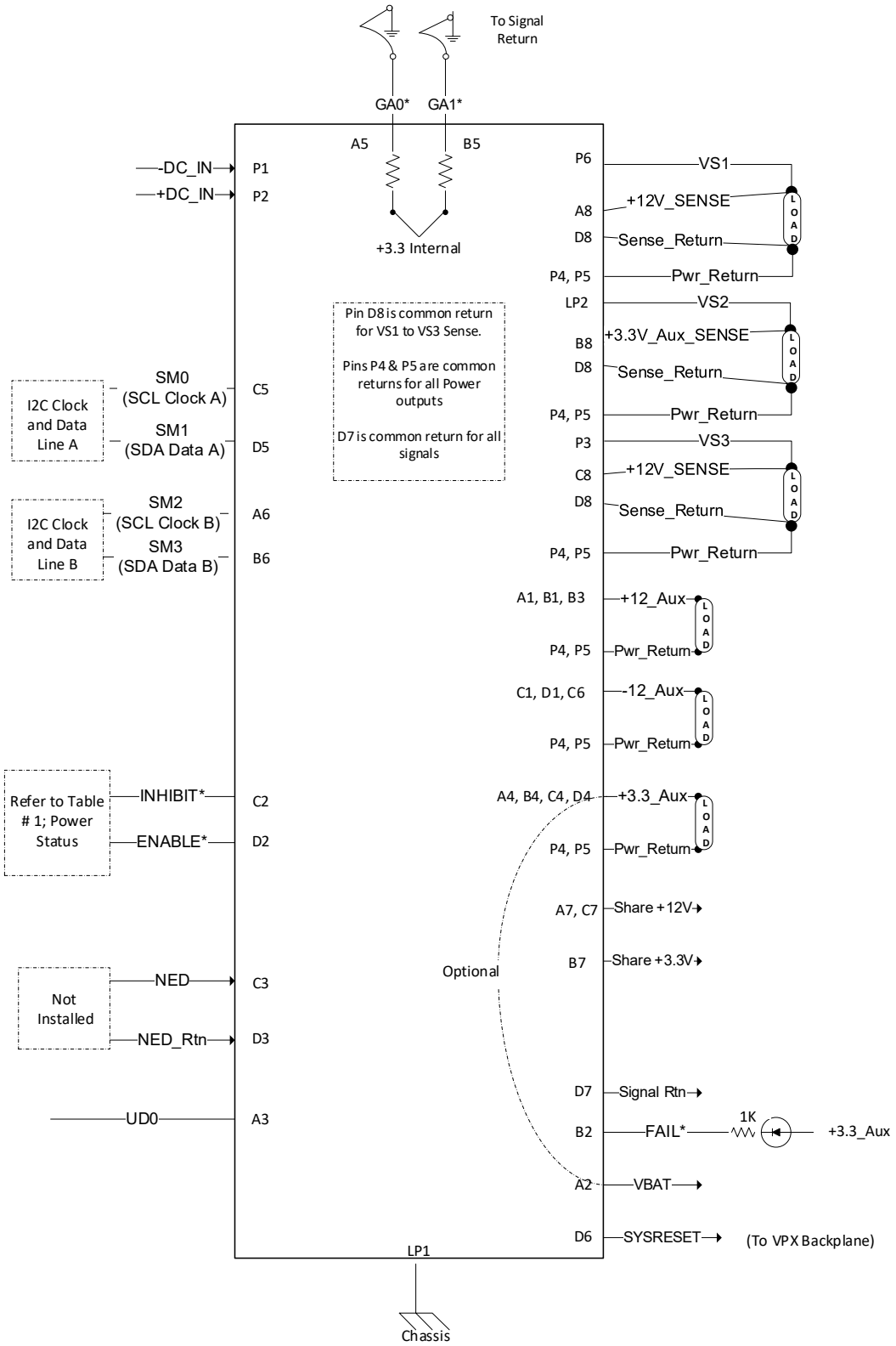
VPX68S Connections



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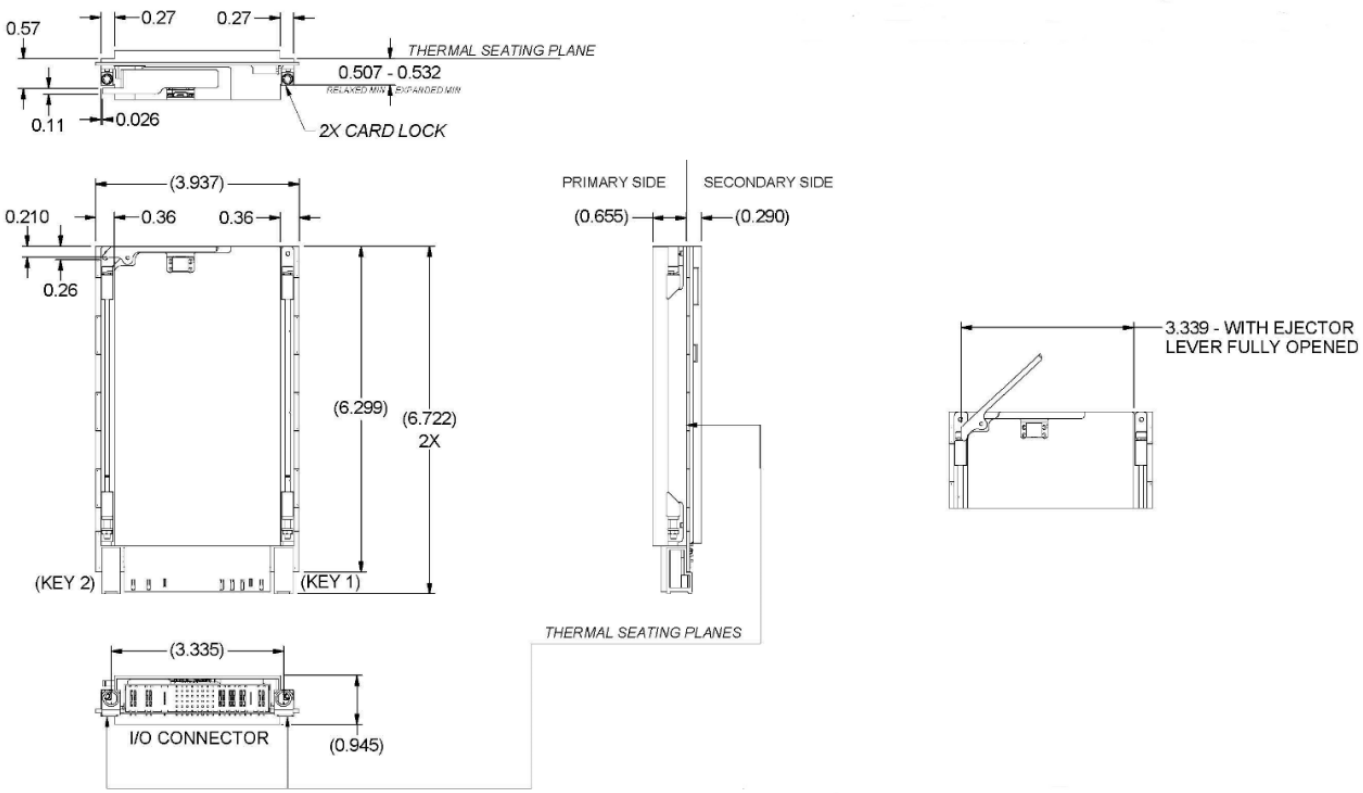
Mechanical Layout



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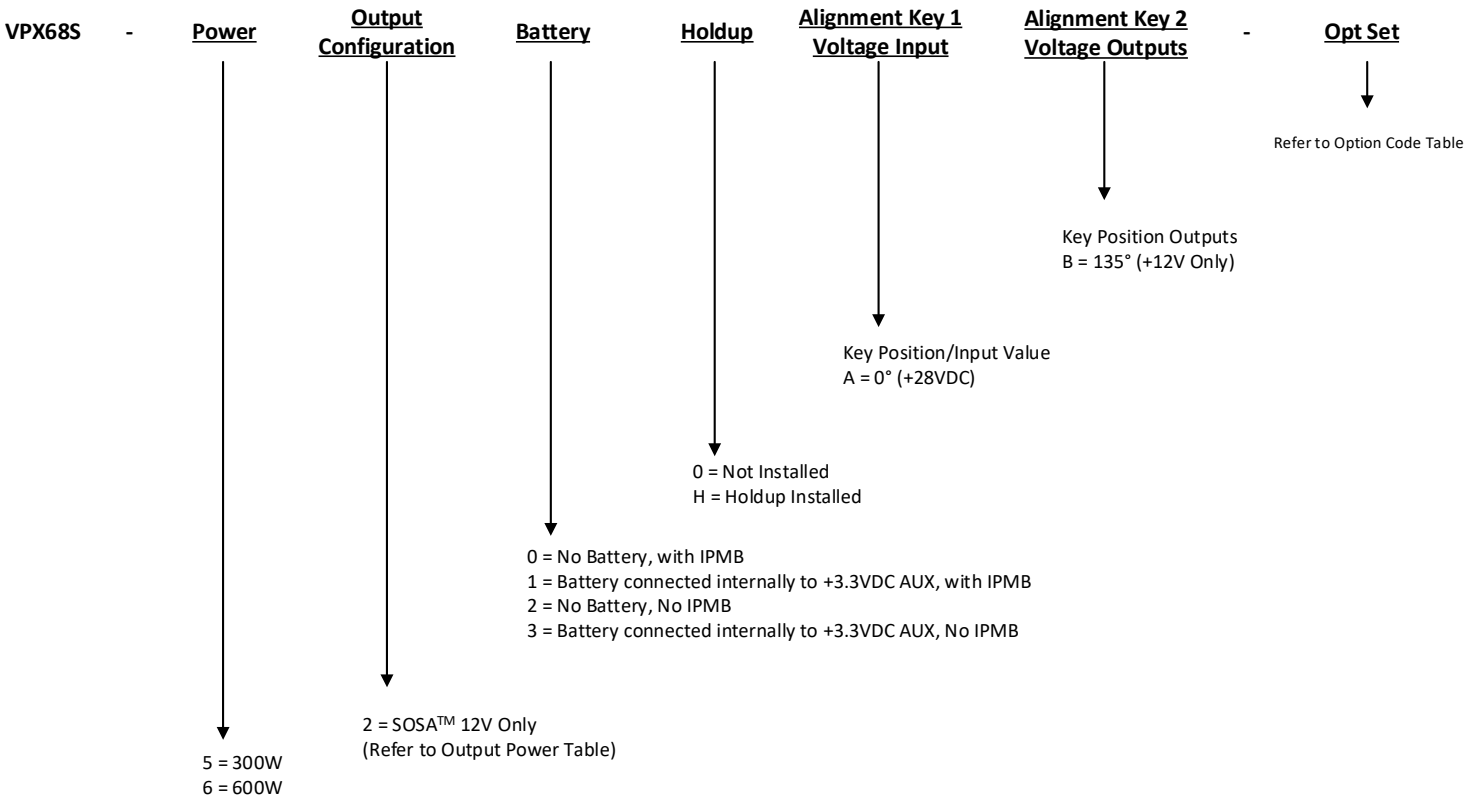
Ordering Information Preliminary



Option Code Table

Code	Description
00	Standard Unit, no additional options
01	Current Share option

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